AMENDMENTS TO THE SPECIFICATION

Paragraph [0007] of the specification is amended to read as follows:

Finally, disclosed herein in another exemplary embodiment is a system for command bus redundancy in a memory subsystem ~~comprising: a means for configuring a memory device array into symbol slices, each symbol slice configured to be part of a single error correction code packet; a means for establishing a plurality of command buses, each command bus configured to interface with each memory device in a particular symbol slice; and a means for configuring a command register with sufficient command bus drivers to support each command bus of the plurality of command buses~~ including a memory device array configured into symbol slices, each symbol slice configured to be part of a single error correction code packet; a plurality of command registers each including a plurality of command buses associated therewith, each command bus configured to interface with each memory device included within a particular symbol slice; and a memory controller, the memory controller in operable communication with the plurality of command registers including a command bus employing an error correction code.

Paragraph [0016] of the specification is amended to read as follows:

Referring now to Figure 3 as well, a simplified block diagram of a single command register ~~42is~~ 42 is depicted. In an exemplary embodiment, SSCR operates by adding additional outputs to the DIMMs command register 42 and corresponding redundant command and address buses 14c. The new outputs are redundant copies that are driven separately to the memory devices 44. In an exemplary embodiment, the copies of the command and address bus 14c are driven to selected memory devices 44 whose data signals are all contained within the same ECC symbol.

Paragraph [0017] of the specification is amended to read as follows:

Advantageously, ~~This~~ this approach constrains the number of redundant outputs of the register 42 and command and address bus 14c lines required, and ensures that any potentially affected data bits are constrained to within the particular ECC symbol. Advantageously, errors within a given ECC symbol are fully correctable by an existing system data ECC. In an exemplary embodiment, memory devices ~~44stacked~~ 44 stacked within a given column (as depicted in Figure 2) are connected together such that they are contained within the same ECC symbol. This is accomplished by ensuring that redundant copies of the command and address bus 14c from the command register 42 correspond to a single data bit ECC symbol. In other words, the memory devices 44 are organized with redundant command and address buses 14c such that each grouping of memory devices is part of a correctable piece of a data word for the given memory subsystem configuration.

Paragraph [0019] of the specification is amended to read as follows:

Turning now to Figure 4, a simplified block diagram depicting the methodology 100 of an exemplary embodiment is depicted. Continuing with process block 102, an array of memory devices 44 are arranged into symbol slices 46 (shown in Figure 2) such that each memory device in the symbol slice is an element of a single error correction code packet. At process block 104, a plurality of command busses 14c is established, where each command bus 14c is configured to drive each memory device 44 of a particular symbol slice as arranged above. Finally, one or more memory register(s) 42 is configured to include sufficient drivers for each command bus 14c established as depicted at process block 106.